IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel Kehrer et al. Examiner: Unknown

Serial No.: 10/520,805 Group Art Unit: Unknown

National Stage Filing Date: January 10, 2005 Docket No.: I432.113.101/P29564

Title: INTEGRATED CIRCUIT ARRANGEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet containing Certificate of Mailing (1 pg.).
- ☒ Information Disclosure Statement (2 pgs.).
- ☒ Form PTO-1449 (1 pg.).
- ☒ Copy of (8) cited references.
- ☒ Return Postcard.

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers, if appropriate. At any time during the pendency of this application, please charge any additional fees or credit overpayment to Deposit Account No. 500471.

Customer No. 025281

By: Steven E. Dicke
Name: Steven E. Dicke
Reg. No.: 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 5 day of April, 2005.

By Steven E. Dicke
Name: Steven E. Dicke

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DM/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel Kehrer et al.	Examiner: Unknown
Serial No.: 10/520,805	Group Art Unit: Unknown
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Title: INTEGRATED CIRCUIT ARRANGEMENT	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached form 1449 be considered by the Examiner and made of record. Any required copies of patents, publications or other documents are enclosed for the Examiner's review. Pursuant to the provisions of M.P.E.P. 609, Applicant further requests a copy of the 1449 form, marked as being considered and initialled by the Examiner, be returned with the next Official Communication.

Since this Information Disclosure Statement is being submitted within three months of filing national application; or date of entry of national application; or before the mailing date of the first Office Action on the merits, a fee has not been enclosed. However, if such fee is required, the Patent Office is hereby authorized to charge Deposit Account No. 500471 for fees as set forth under 37 C.F.R. 1.17(p).

Applicant respectfully requests consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicant's representative at the below-listed telephone number if there are any questions regarding this Communication or the tendered references.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DM/

Information Disclosure Statement
Applicant: Daniel Kehrer et al.
Serial No.: 10/520,805
National Stage Filing Date: January 10, 2005
Docket: I432.113.101/P29564
Title: INTEGRATED CIRCUIT ARRANGEMENT

Respectfully submitted,

Daniel Kehrer et al.,

By their attorneys,

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Telephone: (612) 573-2002
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Dated: April 5, 2005
SED:jan

Steven E. Dicke
Steven E. Dicke
Reg. No. 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 5 day of April, 2005.

By Steven E. Dicke
Name: Steven E. Dicke

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DM/

Receipt date: 04/07/2005

10520805 - GAU: 2817

FORM PTO-1449	Docket No.: I432.113.101/P29564	Serial No.: 10/520,805
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Daniel Kehrer et al.	
	Nat'l Stage Filing Date: 1/10/05	Group Art: Unknown

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
	AA	6,323,735	11/2001	Welland et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub Class	Translated Yes No
	AM	00/51012	08/2000	WO			Yes
	AN	0 574 180	12/1993	EPO			Yes
	AO	0 410 7940	04/1992	EPO			Yes (Abstract Only)
	AP	2809498	03/1978	DE			Yes (Abstract Only)
	AQ	0735656	10/1996	DE			Yes (Abstract Only)
	AR						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AS	Masakazu Yamashina et al., "An MOS Current Mode Logic (MCML) Circuit for Low-Power GHz Processors, NEC Res. & Develop., 36, No. 1 (1995), pp. 54-62.
	AT	Z. Lao et al., "40-Gb/s High-Power Modulator Driver IC for Lightwave Communication Systems, IEEE Journal of Solid-State Circuits, 33, No. 10 (1998), pp. 1520-1526.
	AU	Copy of International Search Report having International Application No. PCT/DE 03/02349 mailed on December 12, 2003.

EXAMINER: /David Mis/ (09/08/2008) DATE CONSIDERED: 09/08/2008

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /DM/